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# MAPLE: Microprocessor A Priori for Latency Estimation

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Saad Abbasi<sup>1</sup>, Alexander Wong<sup>1,2,3</sup>, and Mohammad Javad Shafiee<sup>1,2,3</sup>

<sup>1</sup>Department of Systems Design Engineering, University of Waterloo, Canada

<sup>2</sup>Waterloo Artificial Intelligence Institute, Canada <sup>3</sup> DarwinAI Corp., Canada

## Abstract

Modern deep neural networks must demonstrate state-of-the-art accuracy while exhibiting low latency and energy consumption. As such, neural architecture search (NAS) algorithms take these two constraints into account when generating a new architecture. However, efficiency metrics such as latency are typically hardware dependent requiring the NAS algorithm to either measure or predict the architecture latency. Measuring the latency of every evaluated architecture adds a significant amount of time to the NAS process. Here we propose Microprocessor A Priori for Latency Estimation MAPLE that does not rely on transfer learning or domain adaptation but instead generalizes to new hardware by incorporating a prior hardware characteristics during training. MAPLE takes advantage of a novel quantitative strategy to characterize the underlying microprocessor by measuring relevant hardware performance metrics, yielding a fine-grained and expressive hardware descriptor. Moreover, the proposed MAPLE benefits from the tightly coupled I/O between the CPU and GPU and their dependency to predict DNN latency on GPUs while measuring microprocessor performance hardware counters from the CPU feeding the GPU hardware. Through this quantitative strategy as the hardware descriptor, MAPLE can generalize to new hardware via a few shot adaptation strategy where with as few as 3 samples it exhibits a 3% improvement over state-of-the-art methods requiring as much as 10 samples. Experimental results showed that, increasing the few shot adaptation samples to 10 improves the accuracy significantly over the state-of-the-art methods by 12%. Furthermore, it was demonstrated that MAPLE exhibiting 8-10% better accuracy, on average, compared to relevant baselines at any number of adaptation samples. The proposed method provides a versatile and practical latency prediction methodology inferring DNN run-time on multiple hardware devices while not imposing any significant overhead for sample collection.

## 1 Introduction

In the past decade, deep neural networks (DNNs) have been widely used with great efficacy for a variety of tasks including computer vision [5, 7, 9, 11], natural language processing [8, 15], and speech recognition [6]. However, designing state-of-the-art DNNs is a time-consuming process, often requiring iterative training and validation to ensure the model meets the target accuracy requirements. Furthermore, applications which require on-device inference (e.g. privacy-preserving facial recognition, autonomous driving) exacerbate this process as the task-specific DNNs must now satisfy multiple constraints of energy consumption, inference latency or memory footprint, in addition to just the accuracy.

In recent years, algorithmic solutions such as neural architecture search (NAS) [13, 10, 21, 20, 19, 28, 30] have received significant attention to automatically find Pareto-optimal architectures that achieve superlative efficacy and accuracy simultaneously [26, 29, 16, 27, 33, 25, 36, 24, 37]. The model

efficiency is typically measured via hardware dependent metrics such as architecture latency, memory or energy consumption, which are computationally expensive to acquire. Much of the early work in NAS relied on reinforcement learning [13, 18, 22, 23] which required exorbitant computational resources (e.g. NASNet required 28 days to discover despite using 800 GPUs [13]). The high computational requirements led to efforts which have focused on reducing the cost of running NAS significantly [21, 20, 28]. The state of the art NAS approaches, such as DARTS, can discover optimal architectures in a few hours [20]. Thus, with the latest NAS approaches, the relative cost of measuring architecture latency becomes significant.

Satisfying on-device latency is critical as many applications require real-time inference on the end-device. Since architecture latency is a highly hardware-dependent metric, discovering Pareto-optimal architectures becomes highly challenging due to the diverse number of hardware devices, accelerators and frameworks available for servers and edge devices. To mitigate this issue, some NAS approaches execute the evaluated architectures on the target device to measure the true architecture latency [26]. However, this approach quickly becomes challenging to scale due to i) the large number of architectures that need to be evaluated (e.g. ProxylessNAS evaluates 300,000 architectures in its first round) and ii) the diversity of available hardware (e.g. CPUs, GPUs, ASICs). Therefore, practical hardware-aware NAS necessitates an approach that can mitigate the large sample requirement and enables rapid adaptation to different hardware devices.

Motivated by these challenges, we propose Microprocessor A Priori for Latency Estimation (MAPLE). As shown in Figure 1, MAPLE is a hardware-aware latency predictor based on a novel processor prior modeling strategy for quantitatively characterizing the underlying processor. This hardware descriptor characterizes the target devices’ main processor through vendor-provided hardware performance counters. Performance counters monitor events related to process execution, such as the number of instructions, cycles, branch predictions and cache hits or misses, among hundreds of other similar events. An important consideration here is the availability of performance counters on different hardware. CPU vendors have included performance monitoring units on a wide variety of devices for over a decade [3, 2, 1]. CPU-based performance monitoring is widely used to analyze software performance. In contrast, GPU vendors only support performance monitoring units on a few devices. To avoid being limited by performance-counter availability, MAPLE only relies on microprocessor performance monitoring units. More specifically, MAPLE uses CPU performance monitoring events to characterize GPU hardware by taking advantage of the tight I/O coupling between the CPU and GPU, particularly in latency-oriented applications. This yields a versatile technique that can characterize a wide variety of hardware.

MAPLE measures performance counters while executing all possible operations in the NAS search space. We postulate that characterizing the system hardware at the operator level (rather than at the architecture level) leads to two main benefits. First, even though a NAS search space can create a large number of distinct architectures, the search space is usually comprised of only a few fixed, stable primitive operators with only a few possible parameter choices. The small number of primitive operators results in a relatively small but expressive hardware descriptor, independent of the possible number of architectures in the target search space. Second, since all architectures are comprised of operations from the search space, operator-level characterization would be expressive enough to generalize more effectively to unseen architectures and hardware, yielding higher accuracy while requiring less samples.

Through such operator-level characterization of the hardware, we demonstrate that the proposed MAPLE algorithm adapts to new computing hardware with as few as 3 samples collected from the device. The effectiveness of the hardware descriptor also precludes the need for model adaptation techniques such as meta-learning or transfer-learning. Instead, MAPLE simply relies on mixing the measurements from the new hardware during training.

We demonstrate the adaptive strength of MAPLE on six different devices (3 CPUs and 3 GPUs). To summarize, the key contributions of this study are as follows:

- We introduce a hardware-aware latency predictor based on a novel microprocessor prior modeling strategy for quantitatively characterizing the underlying processor through hardware performance monitoring events.
- By taking advantage of the tight-coupling between a CPU and GPU, we characterize GPU behavior using CPU-based hardware performance counters.

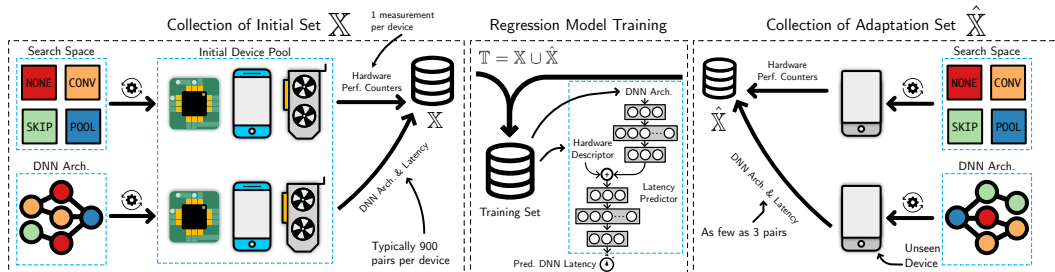


Figure 1: MAPLE overview; MAPLE is a hardware-aware latency predictor capable of inferring DNN architecture latency on new (previously unseen) devices. MAPLE relies on a novel quantitative characterization of the device microprocessor through hardware performance counters. These quantitative metrics characterize the target device based on CPU cache efficacy, computational speed, and memory I/O among other events. MAPLE collects these metrics while executing the NAS search space operations yielding a fine-grained descriptor capable of discerning between different hardware. MAPLE also measures the latency of an initial set of DNN architectures on a set of known devices, enabling generalization on unseen DNN architectures. To adapt to previously unseen hardware, MAPLE characterizes the new hardware through the fine-grained performance metric-based hardware descriptor and measures the latency of just 3 randomly chosen architectures. The few shot adaptation sample efficacy is primarily due to the effectiveness of the quantitative strategy to characterize hardware. The training set is formed by mixing the three adaptation samples into the initial set. The latency predictor is implemented as a neural network-based regression model which is fed DNN architecture encodings and hardware descriptors.

- We propose a simple latency prediction technique that is able to generalize to new hardware with only 3 measurements.
- By characterizing the hardware effectively via the novel approach, we are able to infer latency with higher accuracy while requiring a less diverse hardware pool compared to the state-of-the-art algorithms.

## 2 Related Works

Several research ideas have aimed to alleviate the time and engineering effort required to predict DNN architecture latency on a target computing device. One of the simplest ways to exploit hardware characteristics and use hardware-aware NAS is by employing FLOPs as a proxy for on-device latency estimation [17, 12]. However, FLOPs are in general, too simple of a measure as most deep learning operations are not compute-bound. Thus, FLOPs typically lead to inaccurate estimation of on-device latency. Another simple technique of estimating the latency is by building an on-device latency look-up table (LUT) of all possible operations in a given search space [25, 24, 27, 16]. The NAS then sums the relevant operator latency to estimate the execution time of a given architecture. However, a latency LUT fails to capture the intricacies of architecture optimization (such as layer fusion or I/O optimization) and thus typically exhibits a deviation of 10-20% from the actual end-to-end latency, depending on the underlying hardware and architecture.

A promising approach is to train a regression model on a dataset of architecture and latency pairs, collected from the target device [34, 32, 40]. The regression model can predict the latency of unseen architectures and removes the need to measure the latency of every architecture during the NAS process; significantly decreases the amount of time spent on acquiring latency measurements. This approach results in significantly lower error compared to LUT-based or FLOP-based approaches. However, the regression-model approaches quickly becomes difficult to scale since mandate the NAS algorithm trains a new model for every target hardware, necessitating the collection of a large number of architectures and latency pairs from all target devices.

Building upon latency predictors, Syed and Srinivasan [42] used transfer learning to adapt a regression model to unseen hardware. Although transfer learning reduces the overall cost of sample collection from new hardware, it still requires a considerable number of measurements (i.e. more than 700 samples) from unseen hardware. Towards predicting latency on new hardware, Lee *et al.* [39] employed meta-learning techniques to develop HELP. Similar to our work, HELP adapts a regression model to infer latency on previously unseen hardware. The rapid adaptation is mainly due to the characterization of the hardware using end-to-end latency of reference architectures. Although this technique demonstrates state-of-the-art performance, it requires at least 10 measurements from new

hardware to adapt effectively. Moreover, it requires training samples from a large pool of devices to be effective.

### 3 Methodology

In this section, we formulate the proposed method MAPLE, describe the architecture encoding, and provide details for the hardware descriptor. Our goal is to design a latency estimation inference model capable of generalizing to different hardware by a few shot adaption strategy and acquiring only a few samples from the target device. These few samples serve the purpose of characterizing the new hardware, enabling rapid adaptation.

#### 3.1 Problem Formulation

The latency of a given DNN is a function of the network architecture as well as the underlying hardware executed. Most latency-aware NAS approaches [42, 32] formulate the latency as a function of DNN architecture only. This formulation is typically defined as  $f(\mathbf{a}; \theta) \mapsto \hat{y}$  where  $\mathbf{a}$  is the DNN architecture encoding,  $\hat{y}$  is the inferred latency and  $f$  is a regression model mapping the architectural encoding to inference latency. Subsequently, this approach requires collecting a large number of architecture and latency ( $y$ ) pairs from the target hardware. However, since this regression model is a function of DNN architecture only, it is incapable of adapting to new hardware. Consequently, this approach must collect a large number of architecture latency measurements and train a specific model for every device that the NAS algorithm intends to target for deployment.

To enable rapid adaptation to new hardware devices, the latency model must take into account some hardware characteristics (i.e. be hardware-aware) as prior knowledge. To this end, we formulate the problem of inference latency estimation as a hardware-aware regression model. More formally, the hardware-aware regression model can be defined as  $f(\mathbf{a}, \mathbf{S}; \theta) \mapsto \hat{y}$  where  $\mathbf{S}$  is the quantitative hardware descriptor. The inclusion of  $\mathbf{S}$  ensures that the hardware-aware regression model takes into account not only the architecture distribution but also the hardware distribution, parameterized by  $\mathbf{S}$ , mapping to inference latency. Most hardware-agnostic inference estimation techniques train the regression model on an architecture distribution and subsequently adapt to different hardware through domain adaptation [39] or transfer learning [42]. In contrast, MAPLE generalizes to new hardware at training time via a few shot adaptation strategy where by collecting a small set of adaptation samples, *adaptation set*  $\hat{\mathbb{X}}$ , (i.e., typically as few as three) from every target hardware and mixing them in with the set of available hardware during training, *initial set*  $\mathbb{X}$ . The initial set consists of samples from already seen devices (i.e. the training device-pool) and has considerably more examples compared to the adaptation set (i.e.  $|\hat{\mathbb{X}}| \ll |\mathbb{X}|$ ) and serves the purpose of representing the DNN architectures distribution as well as the hardware distribution. We define the initial set ( $\mathbb{X}$ ) set more formally as

$$\mathbb{X} = \left\{ (\mathbf{a}, \mathbf{S}, y) \mid \mathbf{a} \in \mathbb{A}, \mathbf{S} \in \mathbb{S}, y \in \mathbb{Y} \right\} \quad (1)$$

where  $\mathbb{S}$  is the set of hardware descriptors characterizing every hardware in the training device-pool,  $\mathbb{A}$  is a set of architectures (typically 900) for which we collect the on-device latency,  $\mathbb{Y}$ , from each device in the training device-pool. Similarly, the adaptation set  $\hat{\mathbb{X}}$  can be described as:

$$\hat{\mathbb{X}} = \left\{ (\mathbf{a}, \mathbf{S}, y) \mid \mathbf{a} \in \hat{\mathbb{A}}, \mathbf{S} \in \hat{\mathbb{S}}, y \in \hat{\mathbb{Y}} \right\} \quad (2)$$

where  $\hat{\mathbb{Y}}$  is the measured latency belonging to a set of randomly selected DNN architectures  $\hat{\mathbb{A}}$ , and  $\hat{\mathbb{S}}$  is a set of hardware descriptors characterizing the previously unseen target hardware. The actual training set is then simply  $\mathbb{T} = \mathbb{X} \cup \hat{\mathbb{X}}$ . Since the number adaption examples is considerably less than the number of initial examples, we minimize weighted mean absolute error  $\mathcal{L}$  over the training set  $\mathbb{T}$ :

$$\arg \min_{\theta} = \mathcal{L} \left( f(\mathbf{a}, \mathbf{S}; \theta), w, Y \right) \quad (3)$$

where  $w$  is the assigned sample weight. The adaptation samples are assigned a weight of  $\frac{1}{\sqrt{|\hat{\mathbb{X}}|}}$  and the initial set of examples are assigned a weight of  $\frac{1}{\sqrt{|\mathbb{X}|}}$ . This weighting scheme ensures that the regression model prioritizes the samples from new hardware during training.

The neural network architecture  $\mathbf{a}$  is encoded using a one-hot encoded operations matrix [35] which defines each edge operation in a given architecture. The hardware descriptor  $\mathbf{S}$  is captured by measuring 10 distinct hardware performance counters while executing all possible operations defined in the search space. The hardware descriptor thus effectively carries a unique characterization between the search space and the underlying device.

### 3.2 Dataset and Latency Collection Pipeline

Following experimental setup in BRP-NAS [32] and HELP [39], we use the NAS-Bench-201 dataset [31] for our experiments. NAS-Bench-201 defines 15,625 cell-based DNN architectures. The architectures have a fixed cell topology with five possible operations in its search space including {none, skip-connection, conv1x1, conv3x3, avgpool3x3}. The permissible input and output channels for these operations are 16, 32 and 64, yielding a total of 15 possible variations for the operations can be used in designing a new architectures. To facilitate our experiments, we measure the end-to-end latency of all 15,525 architectures in NAS-Bench-201 on a wide variety of devices. These devices include a 4-core Intel Core i5-7200k, a 12-core Intel i9-9920k, a 20-core Intel Xeon Gold 6230, a 1920-core Nvidia GTX-1070, a 4352-core Nvidia RTX-2080 Ti and finally a 4608-core Nvidia RTX-6000.

In addition to measuring the architecture latency, we also characterize each hardware device by measuring key performance metrics while executing individual operations in the NAS-Bench-201 search space (further details in Section 3.3). More specifically, by employing the Linux performance analysis tool perf [41], we measure key hardware performance metrics while executing each of the 15 operations in the search space. Given that we measure 10 hardware counters per descriptor, the resulting size of the hardware descriptor  $\mathbf{S}$  is 150. In addition to these performance metrics, we also measure the latency of each operation. The rationale for including the operator latency is to allow the model to correlate the end-to-end architecture latency with the operator latency.

### 3.3 Quantitative A Priori Hardware Descriptor

The quantitative a priori model takes advantage of hardware performance counters to characterize a hardware. The hardware performance counters are special-purpose hardware registers within microprocessors that track events related to CPU-cycles, instruction counts, branch mispredictions, and cache miss rates, among other vital low-level metrics. These metrics are widely used for fine-grained performance analysis and for identifying bottlenecks within programs. Performance counters are available on a wide variety of microprocessor architectures [4, 38, 14] and devices. However, performance counters are relatively scarce on GPUs and are only found on select architectures and devices.

Therefore, we avoid using GPU performance events and instead demonstrate that it is possible to predict latency on GPUs while using microprocessor-based counters. The overall GPU performance depends on how fast a microprocessor can continuously keep it fed with data, resulting in tight I/O coupling between the two devices. MAPLE takes advantage of this tight I/O coupling to characterize the GPU while measuring CPU performance counters. This approach yields a versatile hardware descriptor that can be acquired on a wide variety of systems.

We identify ten different hardware performance counters that can characterize the hardware effectively. These counters include CPU-cycles, instructions, cache-references, cache-misses, level one (L1) data cache loads, L1 data cache load misses, last-level cache (LLC) load misses, LLC loads, LLC store-misses and LLC stores. These event counters characterize if a given workload is compute or memory bound, how effectively is the cache utilization and how often the system needs to request data from the main memory.

An important consideration here is the workload executed while the above-mentioned hardware counters are monitored. Some possible options include executing several architectures or a set of reference architectures [39] that can represent the underlying architecture-latency distribution. However, identifying reference architectures becomes challenging as the number of possible architectures allowed by a NAS search space grows. Similarly, the number of architectures that may need to be executed would also increase with the number of possible architectures. In contrast, we propose a more fine-grained approach where we execute all possible operations in a given search space. The advantage offered by this approach is that its independent of the number of architectures and only

depends on the search space size. More importantly, using the entire search space as a workload yields a descriptor that characterizes how the given system behaves with each operator, potentially allowing the regression model to generalize better to new devices.

### 3.4 Regression Model Architecture

The proposed method employs a compact neural network-based non-linear regression model for latency inference. The regression model is hardware-aware and DNN architecture-aware as it accepts the hardware descriptor and DNN architecture encoding as inputs. To cater for the discrete nature of the architecture encoding  $\mathbf{a}$  as well the continuous-valued hardware descriptor  $\mathbf{S}$ , the regression model is designed as a dual-stream neural network architecture (Figure 1 provides an illustration). The first stream takes the architectural encoding as an input and is processed by two hidden layers. The architecture encoding is subsequently mapped to a 32-dimensional continuous space vector before being concatenated with the hardware descriptor  $\mathbf{S}$ . The concatenated vector is the second stream of the regression model consisting of a further two hidden layers. Employing the dual-stream model enables the regression model to learn the characteristics of the architecture encoding and the hardware descriptor independently.

## 4 Evaluation

### 4.1 Experiment setup

In this section, we assess the efficacy of MAPLE against HELP [39] as well as a look-up table (LUT)-based approach as the baseline. We design our experiments specifically to assess three different benchmarks. First, how many samples from the new hardware does the predictor require to outperform the baseline technique? Second, how many devices does the predictor need to see for good generalization? Thirdly, how many samples does the predictor require from each of the devices? These three benchmarks dictate how practical a given latency prediction solution is.

### 4.2 Comparison Metric

Inspired by BRP-NAS [32], we employ error-bound accuracy as our primary metric, which is defined as the percentage of samples that falls within a given error-bound. In this study, we use  $\pm 1\%$ ,  $\pm 5\%$ , and  $\pm 10\%$  error-bounded accuracy. These metrics are widely used in the literature due to their interpretability.

### 4.3 Comparison baselines

We compare the proposed MAPLE against two well-known approaches i) LUT [25, 24, 27, 16] and ii) HELP [39]. Using a LUT for architecture latency yields a simple yet effective approach for estimating how a given architecture would perform on a new device. The number of measurements required depends only on the search space size and not on the number of architectures. Although our experiments showed that the accuracy of a LUT-derived latency depends highly on the complexity of the underlying hardware (see Figure 2), we still consider an architecture latency LUT to be a strong baseline due to its simplicity, relative accuracy and convenience.

HELP [39] is a state-of-the-art method that can generalize to new hardware with as few as 10 samples. The authors demonstrated their technique with seventeen devices and collected 900 training samples. To eliminate any distribution bias, we train HELP and MAPLE on the exact same training samples. Using the same samples ensures that the accuracy results are due to the technique’s ability to generalize to new devices and not due to randomly being trained on a more representative distribution. We modify the HELP implementation to output error-bound accuracy instead of Spearman correlation.

### 4.4 Efficacy of Few shot Adaptation to Unseen Hardware

To compare the efficacy of the proposed approach with the competing methods, we begin by forming a training pool of five devices (mentioned in section 3.2) and using the sixth device for testing purposes. Importantly, we rotate devices into and out of the training pool using leave-one-out cross-validation and average the results. Using leave-one-out cross-validation ensures that the results are invariant of

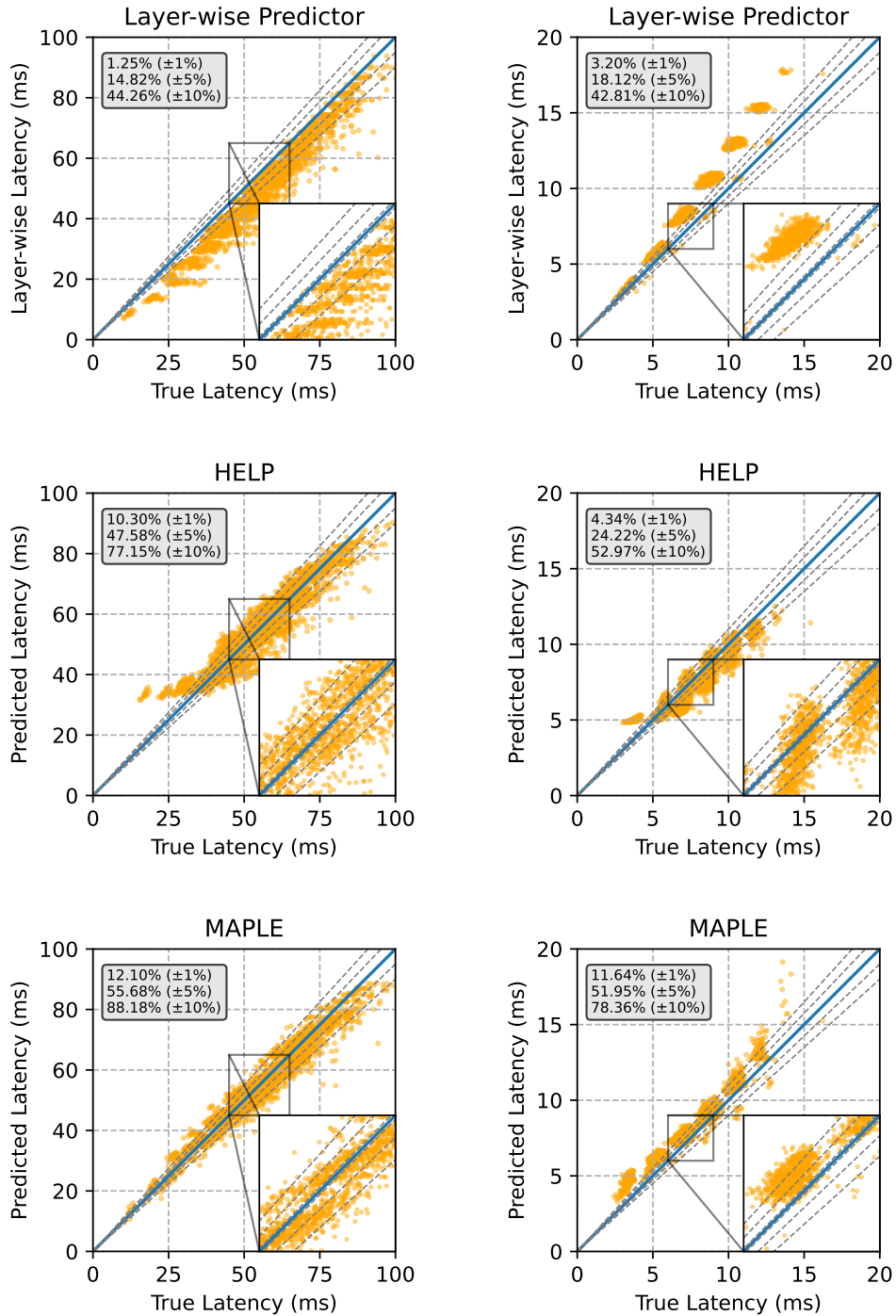


Figure 2: Visual comparison of true and predicted latency on Intel Xeon Gold 6230 and Nvidia RTX6000. The HELP and MAPLE methods were trained on 900 samples collected from each of the five devices in the training pool. The MAPLE method was adapted by mixing in 3 samples whereas the HELP method was adapted using 10 samples. The blue line represents perfect prediction accuracy whereas the dashed gray lines represent  $\pm 1\%$ ,  $\pm 5\%$  and  $\pm 10\%$  error bounds. The error-bound accuracy for each technique is annotated in the top left corner. The insets provide a closer comparison of where each technique places the predicted latency. For example, HELP is able to place a significant number of points within  $\pm 5\%$  error but exhibits a considerable bias (many points are above the blue line). In contrast, MAPLE distributes the predictions within  $\pm 5\%$  more evenly and is thus able to deliver an accuracy of 71.49%.

Table 1: Comparison of few-shot adaptation efficacy between HELP and MAPLE. Both techniques were trained with 900 points from each of the five hardware devices in the training device-pool. HELP was adapted to the unseen devices by collecting 10 additional samples as suggested by the authors [39]. The efficacy of MAPLE is demonstrated by mixing 3 as well as 10 samples. The reported metric is  $\pm 10\%$  error-bound accuracy. We note that although MAPLE benefits from mixing in 10 samples, mixing only 3 samples also outperforms HELP algorithm and provides a 3% improvement over HELP.

Method	No. of Samples	Unseen CPU			Unseen GPU			Mean
		i5-7600k	i9-9920k	Xeon 6230	GTX1070	RTX2080	RTX6000	
HELP	10	0.93	0.93	0.77	0.95	0.75	0.53	0.81
MAPLE	3	0.85	0.94	0.88	0.90	0.75	0.78	0.85
MAPLE	10	0.99	0.96	0.92	0.99	0.95	0.83	0.94

a specific device combination. We train both HELP and MAPLE using the same 900 training samples per device and validate using all 15,625 architectures in NAS-Bench201. Table 1 shows a detailed comparison between HELP, the LUT baseline and our method. To stay consistent with the original study, we use 10 samples to adapt HELP to test devices [39]. To demonstrate the hardware adaptation capability of MAPLE, we evaluate our method with as few as 3 samples as well.

Table 1 compares the 10% error-bound accuracy between HELP and MAPLE. This Table illustrates MAPLE’s efficacy in rapid model adaptation. We note that MAPLE reports an improvement of 3% despite using only 3 samples for model adaptation compared to HELP’s 10 samples. Moreover, we note that when MAPLE uses 10 adaptation samples, the performance improves significantly from an average of 0.85% to 0.94%. Importantly, our regression model was adapted to GPUs presented in Table 1 using CPU-based performance counters. The model is able to adapt to GPUs with only 3 samples due to the tight-coupling present between the CPU and GPU, as discussed in Section 3.3. This illustrates the effectiveness of using widely available CPU performance counters to characterize GPU hardware.

Figure 2 provides an illustrative comparison between the architecture layer-wise predictor, HELP and MAPLE. The blue line in the Figure serves as a guide for perfect prediction latency while the dashed gray lines visually show the  $\pm 1\%$ ,  $\pm 5\%$ , and  $\pm 10\%$  error bounds. We again use 10 samples with HELP and 3 samples with MAPLE for model adaptation. In Figure 2 (top left) we show the correlation between the true latency and summed layer-wise latency. The layer-wise latency was computed by summing the execution time of all primitive operations that a given architecture was comprised of. Each sample was measured 25 times and averaged to get a robust estimate. We note that the layer-wise predictor consistently underestimates the architecture latency with the error growing for higher latency models. This illustrates that simply summing the operator latency fails to capture the intricacies of running a full DNN architecture. Employing HELP (top center) reduces the error significantly, with most architectures falling within  $\pm 10\%$  of the actual latency. In contrast, MAPLE is able to outperform HELP and exhibits an improvement of nearly 10%, while utilizing only three samples for model adaptation. We observe a similar trend when assessing the plots for Nvidia RTX6000 GPU. The layer-wise predictor consistently overestimates the architecture latency. HELP again closes the gap between the predicted latency but generally underestimates the architecture latency for a significant number of samples. In comparison, MAPLE can bring over half the points within  $\pm 5\%$  error while employing just three points.

#### 4.5 Hardware Adaptation Efficiency

In this experiment, we explore how many samples MAPLE requires to adapt to previously unseen hardware. We fix the number of training samples per device to 900 and form a training pool of 5 devices. Like Section 4.4, we employ one-leave-out cross-validation to rotate through the test devices and average the resulting 10% error-bound accuracy. We evaluate HELP and MAPLE over a range of 2 to 20 adaptation samples. To provide experimentally robust results, we performed the experiment with five random seeds and averaged the results. As we want to investigate the hardware adaptation efficiency, we aggregate the results by device type (CPU or GPU), as shown in Figure 3 (left). We note that the accuracy for both approaches rapidly increases until 10 adaptation samples, after which it flattens out. However, MAPLE largely outperforms HELP on both CPU and GPU hardware, averaging an improvement of 8-10%. This difference in adaptation efficiency can likely be



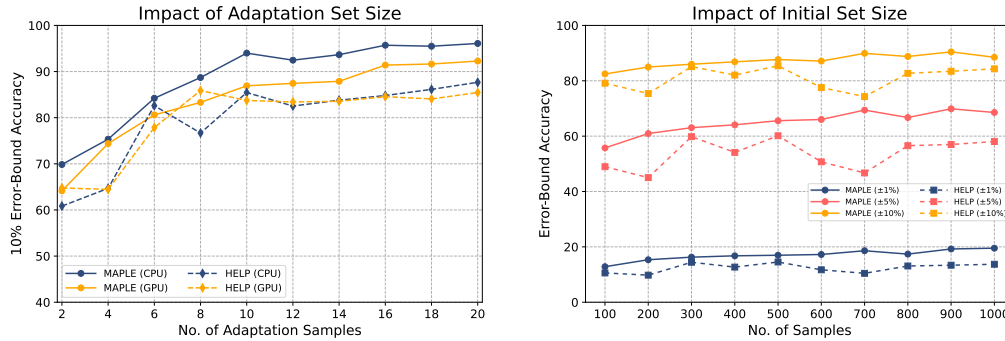


Figure 3: (left) Impact of number of adaptation samples in MAPLE and HELP, aggregated by the device type. Each combination of the training pool was tested by leave-one-out cross-validation. To ensure the results are robust, measurements were taken across 5 different seeds for each assessment and averaged. (right) Impact of the size of the initial set ( $\mathbb{X}$ ) on MAPLE and HELP, aggregated by error-bound accuracy. Each combination of the training pool was tested by leave-one-out cross-validation. To ensure the results are robust, measurements were taken across 5 different seeds for each assessment and averaged. Interestingly, MAPLE exhibits flatter but higher accuracy curves. This suggests that MAPLE is able to generalize to unseen DNN architectures through fewer training examples, reducing the time required to collect datasets from different hardware significantly.

explained by the fact that HELP uses references architectures for hardware generalization. However, optimal reference architectures likely depend on the device pool as well as the search space. In contrast, MAPLE is able to generalize to new hardware through randomly selected architectures.

#### 4.6 Impact of Training Set Size

The number of training examples directly impacts the cost that a latency predictor incurs on a NAS process and is a crucial indicator of its practicality. We, therefore, assess how many training examples MAPLE need to see before generalizing well to a new device. In this experiment, we fix the number of adaptation samples to 3 for MAPLE and 10 for HELP. As before, we use leave-one-out cross-validation to test every possible combination of training devices and average the results across the 6 test devices. We vary the number of training examples from 100 to 1000 and measure the test accuracy with all 15,625 architectures present in NAS-Bench201. As the goal of this experiment is to assess the impact of number of training examples on the accuracy, we plot  $\pm 1\%$ ,  $\pm 5\%$  and  $\pm 10\%$  error bound accuracy for HELP and MAPLE (Figure 3 (right)). We note from the Figure that MAPLE outperforms HELP throughout the sample range. Surprisingly, the accuracy trend is relatively flat, indicating that MAPLE does not require a large number of training samples for efficacious generalization. Importantly, the low sample requirement implies that MAPLE does not require significant training time. Even with a total of 4,500 samples (900 per device), the training time on an Nvidia GTX1070 was only 90 seconds. This implies that MAPLE can be re-trained at will with a different device pool if required with no significant overhead.

#### 4.7 Conclusions

In this work, we proposed MAPLE, a simple yet effective latency predictor that is able to rapidly adapt to new hardware. MAPLE is based on a novel device descriptor that is able to characterize the target hardware by measuring ten key performance metrics, including cache efficacy, computational rate and instruction count, among others. These metrics are captured by measuring key CPU-based hardware performance counters while executing key primitive workloads on top. Hardware performance counters yield an efficient hardware descriptor that enables MAPLE to generalize to new devices with as few as three samples. Moreover, the proposed hardware descriptor is also able to characterize GPUs despite being based on CPU-based hardware performance counters. The GPU characterization is possible as the proposed technique takes advantage of the tight-coupling present between the CPU and GPU. In contrast to other approaches which use fine-tuning or meta-learning, we incorporated the target device characterization at training time, yielding a simple yet accurate approach to latency prediction. We validated MAPLE by conducting a series of experiments. First, we assessed the latency prediction accuracy on new hardware with as few as three and ten samples. Employing just three adaptation samples yielded a 3% improvement over the state of the art while using ten samples yielded

an improvement of 12%. Second, we assessed how many samples the proposed method requires to generalize effectively to new devices. We found that MAPLE yielded an average improvement of 8-10% over other approaches. Finally, compared to the state-of-the-art techniques, MAPLE also requires significantly fewer training examples to generalize to unseen network architectures. These characteristics yield a simple latency predictor that can significantly reduce the cost hardware-aware NAS.

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